**Progress Report**

L2 unified cache and branch prediction are completed by checkpoint 3, but data forwarding has not been completed although it works for some parts. Mike was doing on his part, but he couldn’t finish on time, so other members hoped in, and yet working on it. Preparing on upcoming checkpoint is almost done since EWB design is basically done, while HW prefetching and pipelined cache design are still on the working progress.

**Advanced Features recommended and planned**

1. HW based prefetching

- As of our discussion, we know that this can be done by adding some modules only, such as adding stream buffers, and prefetching signals so it can prefetch data/instruction into stream buffers while execution

- stream buffer between L1 cache and L2 cache

2) EWB (single cacheline) or victim cache(cache holding multiple cachelines) paralyzing the WB.

- almost done drafting EWB so may go with EWB

- upon a WB, writeback request to EWB, not our next level of memory. Then it services the writeback at next available opportunity when the next level cache is free

- load should only stall if there is a WB performed while EWB is full.

1. pipelined cache

**Roadmap**

04/20: finishing up checkpoint 3 / preparation of upcoming checkpoints

04/21: Begin writing EWB and HW prefetching, share ideas about these along with pipelined cache

04/22: design on pipelined cache should be completed. Connecting EWB and HW prefetching has to be done mostly / TA meeting

04/23: Pipelined cache progress (1/2), CP progress report starts

04/24: Pipelined cache progress (2/2), CP progress report almost completed without a part related to Pipelined cache

04/25: Debugging

04/26: Debugging

04/27: CP4 due and CP5 is due in two more days so wrapping up all the parts we have thought missing or planned to add.

04/28: Debugging, presentation and final report preparation

04:29: Debugging and wrap up MP3